AF/2841

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Goruganthu et al.	Examiner:	Souw, B.
Serial No.:	09/583,617	Group Art Unit:	2881
Filed:	May 31, 2000	Docket No.:	AMDA.441PA
Title:	ELECTRICAL PROBING OF SOI CIRCUITS		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited, **in triplicate**, in the United States Postal Service, as first class mail, in an envelope addressed to: Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on June 30, 2003.

By: _____
Name: Erin M. Nichols

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
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Sir:

This is an Appeal Brief submitted pursuant to 37 C.F.R. § 1.192 for the above-referenced patent application. Please charge Deposit Account 01-0365 (TT3751) in the amount of $320 for this brief in support of appeal as indicated in 37 C.F.R. § 1.17(c). If necessary, authority is given to charge/credit Deposit Account 01-0365 (TT3751) any additional fees/overages in support of this filing.

I. Real Party in Interest

The real party in interest is Advanced Micro Devices, Inc. (AMD), of Sunnyvale, CA. The above-referenced patent application is assigned to AMD.

II. Related Appeals and Interferences

There are no related appeals or interferences.

III. Status of Claims

Claims 1-19 and 21-29 are presented for appeal. Claims 28 and 29 stand rejected under 35 U.S.C. § 112(1) as containing subject matter not described in the specification; claims 1, 2, 8-11 and 16-19 stand rejected under 35 U.S.C. §§ 102(a) and 102(e) as being clearly anticipated by *Yoshida* (U.S. Patent No. 6,137,295); claims 3-7, 12, 13 and 21-23 stand rejected under 35 U.S.C. §§ 102(a) and 102(e) as being anticipated by *Yoshida*; claim 13 stands rejected under 35 U.S.C. § 103(a) as being obvious over *Yoshida*; claim 14 stands rejected under 35 U.S.C. § 103(a) as being obvious over *Yoshida*; claims 24-27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yoshida*; claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yoshida*; and claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yoshida* in view of *Talbot et al.* (U.S. Patent No. 6,019,249) and *Steffan et al.* (U.S. Patent No. 6,200,823). The pending claims presented for appeal, as presently amended, may be found in the attached Appendix of Appealed Claims.

IV. Status of Amendments

The application was originally filed on May 31, 2000, including 23 claims. In reply to a first Office Action mailed on August 30, 2002, an Office Action Response was filed on November 26, 2002, including, *inter alia*, the cancellation of claim 20. On January 29, 2003, a final Office Action was mailed, and in reply, a Final Office Action Response was filed via facsimile on March 31, 2003, including, *inter alia*, an amendment to the specification and the addition of new claims 24-29. A Notice of Appeal was filed via facsimile on April 29, 2003. A second final Office Action was mailed on May 9, 2003 indicating that the grounds of rejection were "repeated without any change in this new Final Office Action." In reply to the second final Office Action, a Supplemental (Communication Regarding) Notice of Appeal was filed via facsimile on May 19, 2003.

V. Summary of the Invention

The present invention is directed to a method for analyzing a flip-chip semiconductor die having silicon-on-insulator (SOI) structure by inducing and detecting a response from an exposed region of the die. A portion of the back side substrate is removed in order to expose a

portion of the insulator layer. The response is detected from the exposed region as a function of a portion of the circuitry which is then used to analyze the die.

One embodiment of the present invention is directed to a method for analyzing a semiconductor die having SOI structure and a back side opposite circuitry near a circuit side. Substrate is removed from the back side of the semiconductor die and a region of the insulator of the SOI structure is exposed where the substrate was removed. A detectable response is then induced from the exposed region as a function of a portion of the circuitry from which the die is analyzed.

Another embodiment of the present invention is directed to analyzing a semiconductor die having SOI structure and a back side opposite circuitry near a circuit side using electrical signals. Substrate is removed from the back side of the semiconductor die and a region of the insulator of the SOI structure is exposed where the substrate was removed. Electrical signals are input to the die to operate the die in a continuous loop known to cause a failure in a portion of circuitry in the die. An electron beam is then directed to the exposed region of the insulator and a detectable response is induced therefrom as a function of the portion of the circuitry failing. The die is then analyzed.

Another embodiment of the present invention is directed to a system for analyzing a semiconductor die having SOI structure and a back side opposite circuitry near a circuit side. The system includes a substrate removal arrangement adapted to remove substrate from the back side of the semiconductor die and expose a region of the insulator of the SOI structure where the portion has been removed. The system also includes a probe arrangement adapted to induce a detectable response from the exposed region as a function of the circuitry and a detector adapted to detect the response and, therefrom, analyze the die.

VI. Issues for Review

Issue 1: Should the Section 102 and Section 103 rejections of the appealed claims be maintained when the cited references fail to teach or suggest every limitation of the appealed claims?

Issue 2: Should the Section 103 rejections of the appealed claims be maintained when the evidence of record shows that there is no motivation for modifying the primary '295 reference?

Issue 3: Should the Section 112(1) rejection of claims 28 and 29 be maintained when the Specification teaches the subject matter of these claims including "logic states" and "circuit nodes"?

VII. Grouping of Claims

The claims as now presented do not stand and fall together and are separately patentable for the reasons discussed in the Argument. For purposes of this appeal, the claims should be grouped as follows: Group I - claims 1, 2, 4-13, 16-19 and 23; Group II – claim 15; Group III – claims 3, 21 and 22; Group IV – claims 14 and 24-27; and Group V – claims 28 and 29.

VIII. Argument

Appellant submits that the claims of groups I – V are patentably distinguishable from each other and from the cited prior art references. The claims in group I are patentable over the prior art, because they are directed to subject matter that includes a method for analyzing a semiconductor die having silicon-on-insulator (SOI) structure including inducing a detectable response from an exposed region as a function of a portion of the circuitry, which is not taught or suggested by any of the references cited. The claim of group II is separately patentable over the other claim groups because it is directed to subject matter that includes inducing a detectable response from a non-defective die, which is not necessarily present in the other claim groups and not taught by the cited prior art. The claims of group III are separately patentable over the other claim groups because they are directed to subject matter that includes using a scanning electron microscope, which is not necessarily present in the other claim groups and not taught by the cited prior art. The claims in group IV are separately patentable over the other claim groups because they are directed to subject matter that includes inputting signals in a continuous loop, which is not necessarily present in the other claim groups and not taught by the cited prior art. The claims in group V are separately patentable over the other claim groups because they are directed to subject matter that includes logic states and a plurality of circuit nodes, which is not necessarily present in the other claim groups and not taught by the cited prior art.

The Office Action dated May 9, 2003 indicated that claims 21-29 have been entered and are rejected therein. This Appeal Brief refers to the Office Action dated May 9, 2003 unless otherwise noted.

Issue 1: The Section 102 and Section 103 rejections of the appealed claims should be reversed because the cited references fail to teach or suggest every limitation of the appealed claims.

The present invention is generally directed to a method of analyzing a semiconductor die having SOI structure, the method including, *inter alia*, exposing a region of the insulator in the SOI structure and inducing a detectable response from that exposed region of insulator, *e.g.*, as in claim 1. In contrast, the '295 reference teaches removing the SOI insulator layer (as shown with insulator 1c removed at opening 1j of Fig. 5), to expose directly "wires on the surface of an integrated circuit [. . .] from the rear side." Col. 6, lines 32-37; 58-60. The exposed wires are then directly accessed (optically) "because no secondary electrons are accumulated in an insulating layer 1c" (Col. 6, lines 54-56). Thus, because the insulator layer is removed, the '295 reference fails to teach inducing a detectable response from the exposed region of insulator as claimed by Appellant. Each of independent claims 1, 16, and 17 include these and other distinguishing limitations and therefore, each of the prior art rejections (under sections 102 and 103) should be removed.

This point is readily recognized by comparing Appellant's claim 1 to the cited teaching of the '295 reference. Claim 1 of Appellant's specification includes, among other aspects, "exposing a region of the insulator of the SOI structure where the substrate has been removed; and inducing a detectable response from the exposed region [of the insulator]." The Office Action dated May 9, 2003 cites the Figure 5 discussion of the '295 reference (at column 6) wherein the reference explains that "a potential contrast image can be easily viewed . . . because no secondary electrons are accumulated in an insulating layer 1c" (Column 6, lines 52-55).* No secondary electrons are accumulated in the insulating layer 1c because the insulating layer 1c is no longer there: "the insulating layer 1c is removed" (Column 6, lines 58-59). Thus, because the insulating layer 1c is no longer there, the assertion that that the '295 reference teaches "inducing a detectable response from the exposed region [of the insulator]" is wrong.

With respect to the rejection of claim 13, the Office Action indicates at page 21 that "the step of 'inputting a signal (through the DUT board 12) known to induce a failure in the die' is not explicitly recited" in the '295 reference. This admission of a lack of correspondence to the present

* At paragraph 23 (page 16) of the Office Action, the Examiner offers an alternative theory for rejecting the claims contingent on an unrealistic and unacceptable interpretation by Appellant.

invention renders the Section 102 rejection of claim 13 improper. Further, the Office Action proposes modifying the '295 reference only to "input a signal through the DUT board 12 until a failure is induced in the die" which is not equivalent to the claimed invention's "inputting signals known to induce a failure in the die." The Office Action fails to present references that teach or suggest all of the claimed limitations and fails to propose modifying the cited references to correspond to the claimed invention.

With respect to the rejection of claims 14 and 24-27, the Office Action acknowledges at page 23 that the '295 reference fails to teach limitations regarding inputting signals in a continuous loop. In an attempt to overcome this deficiency, the Office Action erroneously asserts that inputting signals in a continuous loop "is normally implemented manually." This is untrue. The speed at which the claimed intricate semiconductor circuitry operates renders a manual input of signals impractical. The circuitry is operated with a continuous loop in order to monitor the changing response of the die. The Office Action fails to present any evidence of motivation, or even any references, for modifying the '295 reference to correspond to the claimed invention, therefore, the Section 103 rejection cannot be maintained.

The Section 102 rejection of claims 3, 21 and 22 should also be reversed because the Office Action also fails to cite a reference that teaches or suggests all of Appellant's claimed limitations. These claims include analyzing the die using a scanning electron microscope (SEM). In a failed attempt to overcome the lack of prior-art correspondence, the Examiner attempts to establish an inherency argument. The '295 reference fails to teach the use of a SEM. The Office Action, at page 8, asserts that a SEM is inherent to the '295 teachings by alleging that a SEM "is *any* device that is capable of performing the following functions, (a) electron beam (EB) irradiation, (b) detecting secondary electrons generated by the EB on the sample, (c) scanning the EB to generate an image, (d) having resolution capability of microscopic scale (e.g., transistor details), and . . . (e) an image-magnifying capability." The Examiner does not provide any support for these criteria, the criteria fail to satisfy the requisite evidence to establish inherency, and the Examiner's unsupported rationale contradicts well-established scientific treatises.

To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter *is necessarily present in the thing described in the reference*, and that it would be so recognized by persons of ordinary skill." Continental Can Co. v. Monsanto Co., 948 F.2d 1264, 1268, 20 U.S.P.Q.2d 1746, 1749 (Fed. Cir. 1991) (emphasis added). "Inherency, however,

may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Id.* at 1269, 20 U.S.P.Q.2d at 1749 (quoting In re Oelrich, 666 F.2d 578, 581, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981). The Examiner's criteria are also applicable to a transmission electron microscope as evidenced by the enclosed pages from the well-known treatise, Stanley Wolf Ph.D. and Richard N. Tauber Ph.D., Silicon Processing for The VLSI Era, Vol. 1, 1986, pages 592-599. Therefore, in addition to the Examiner's rationale being misplaced, this rationale does not support the proposition that the '295 reference is inherently teaching a SEM.

In furtherance of this misplaced rationale, the Examiner erroneously cites claims 2, 6, 8 and 10 of the '295 reference as corresponding to a SEM. Rather, claims 2, 6, 8 and 10 are directed to directly accessing the insulator-exposed wires (Fig. 5) using a conductive ("probe") needle that is connected to a probe card (Col. 9, lines 26-36) for use with an infrared camera 40; these claims are therefore inapplicable to Appellant's claimed invention involving a SEM. Since other devices could satisfy the Examiner's criteria, it is not inherent that the '295 reference teaches a SEM and therefore, does not completely correspond to Appellant's claimed invention. Without complete correspondence, the §102 rejection cannot be maintained.

Issue 2: The Section 103 rejections of the appealed claims should be reversed because the evidence of record shows that there is no motivation for modifying the primary '295 reference.

Each of the Section 103 rejections relying on the modification of the '295 reference is improper because the Examiner failed to establish obviousness. In order to establish a *prima facie* case of obviousness, in addition to the Office Action presenting a teaching of prior art references so as to provide complete correspondence to the claimed invention, there must also be evidence of motivation for combining the prior art references as asserted. The Office Action also fails to meet the motivation requirement.

Accordingly, the Section 103 rejections should also be reversed because the Examiner failed to cite motivation in support of the asserted modifications of the primary '295 reference. A Section 103 rejection requires that an asserted modification of a reference relied upon in making the rejection must be motivated, and that motivation must be supported by evidence found in the prior art. *See, e.g.,* In re Dembiczak, 175 F.3d 994, 50 U.S.P.Q.2d 1614 (Fed. Cir.

1999). Recent case law has also explicitly defined that the motivation criterion for a Section 103 rejection requires evidence that must be specifically identified and shown by some objective teaching in the prior art leading to the modification. Specifically, "[o]ur court has provided [that the] motivation to combine may be found explicitly or implicitly: 1) in the ***prior art references*** themselves; 2) in the knowledge of those of ordinary skill in the art that certain ***references***, or disclosures in those references, are of special interest or importance in the field; or 3) from the nature of the problem to be solved, 'leading inventors to look to ***references*** relating to possible solutions to that problem.'" Ruiz v. A.B. Chance Co., 234 F.3 654, 57 U.S.P.Q.2d 1161 (Fed. Cir. 2000). As evidenced by a careful review of the Office Action, the Examiner has failed to cite any specific portions of the prior art that would lend support for the rationale for the asserted modification.

Generally, the concept of modifying Fig. 5 of the '295 reference so as to correspond with the claimed invention would require not removing the insulator. However, not removing the insulator would frustrate the purpose of observing a potential waveform with high precision because secondary electrons would accumulate in the insulating layer. Col. 6, lines 54-55. Thus, the '295 reference directly teaches away from any such modification. *See,* In re Gordon, 733 F.2d 900 (Fed. Cir. 1984) (a §103 rejection cannot be maintained when the asserted modification undermines purpose of main reference).

With respect to the rejection of claim 15, the Office Action fails to identify any evidence of factual teachings, suggestions or incentives from the '295 reference for why one skilled in the art would be led to modify the '295 reference. The Examiner's citation of the '823 reference only recites rationale behind comparison between a defective and non-defective die in the context of that reference; no mention is made as to why one of skill in the art would modify the '295 reference in this manner. Specifically with respect to claim 15, the '295 reference plainly teaches various methods for detecting defects without using a non-defective die; indeed, these various methods are recited as specific "objects" of the invention. *See, e.g.,* column 3, lines 38-55. For example, the '295 reference teaches away from such a comparison because it positively identifies the location and uses specific test signals as recited in column 6, lines 33-34, indicating that "it is necessary to designate a location to be observed." Therefore, one of skill in the art would not be motivated to modify the '295 reference to include limitations directed to a comparison to a reference die.

As provided by long-standing case law, where the proposed modification to the main prior art reference would undermine the purpose or "object" of the invention, the main prior art reference teaches away. *See,* In re Gordon.

In view of the above, the Examiner failed to identify evidence that shows how the prior art (rather than the Examiner's arguments) would lead one skilled in the art to modify the '295 reference. No evidence of factual teachings, suggestions or incentives from the prior art that lead to the proposed modification has been cited. Therefore, the motivation requirement for establishing a *prima facie* case of obviousness has not been met, and Appellant submits that the Section 103 rejections must be reversed.

Issue 3: The Section 112(1) rejection of claims 28 and 29 should be reversed because the Specification teaches the subject matter of these claims including "logic states" and "circuit nodes".

The Office Action asserts that the Specification does not describe "logic states" or a "plurality of circuit nodes." Current case law states that, "The written description requirement does not require the applicant "to describe exactly the subject matter claimed, [instead] the description must clearly allow persons of ordinary skill in the art to recognize that [he or she] invented what is claimed."" Union Oil Co. of California v. Atlantic Richfield Co., 208 F.3d 989 (Fed. Cir. 2000), *cert. denied*, 69 U.S.L.W. 3165 (Feb. 20, 2001) (No. 00-249) (quoting In re Gosteli, 872 F.2d 1008, 1012, 10 U.S.P.Q.2d 1614, 1618 (Fed. Cir. 1989) (citations omitted)). Furthermore, neither the rules nor the law require word-for-word support in the detailed description. In re Wertheim, 541 F.2d 257, 265, 191 U.S.P.Q. 90 (CCPA 1976); MPEP § 2163.02.

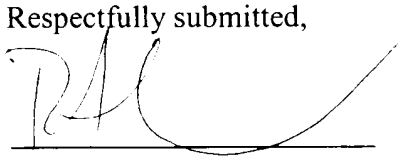
With respect to "logic states", page 6, lines 4-6 of the Specification teaches, "The analysis can be used, for example, to determine die logic states for post-manufacturing analysis." Subject matter relating to "logic states" is clearly discussed in the Specification. With respect to the limitations regarding circuit nodes, Appellant submits that the detailed description throughout discusses circuitry and portions of circuits and that one skilled in the art would recognize that any such circuit or circuitry inherently contain nodes. A node is a junction or branch point in a circuit. *See*, http://www.twysted-pair.com/dictn.htm. One skilled in the art of post-manufacture flip-chip semiconductor die circuit failure analysis would readily recognize the circuit features (*e.g.*, logic states and circuit nodes) being analyzed in conjunction with the claimed invention.

IX. Conclusion

In view of the above, Appellant believes the claimed invention to be patentable and that the rejections of claims 1-19 and 21-29 must be reversed. Appellant respectfully requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the Assignee's deposit account was provided on the first page of this brief.

Respectfully submitted,



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APPENDIX OF APPEALED CLAIMS

1. A method for analyzing a semiconductor die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side, the method comprising:

removing substrate from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure where the substrate has been removed; and

inducing a detectable response from the exposed region as a function of a portion of the circuitry and, therefrom, analyzing the die.

2. The method of claim 1, wherein inducing a detectable response includes using an electron beam.

3. The method of claim 2, further including detecting secondary electrons generated in response to the electron beam and the portion of the circuitry and wherein analyzing the die includes using a scanning electron microscope (SEM).

4. The method of claim 3, wherein analyzing the die includes detecting a first magnitude of secondary electrons from a selected circuit portion and a second magnitude of secondary electrons detected from another circuit portion, the first and second magnitudes of secondary electrons being indicative of an electric characteristic differential between the selected circuit portion and the other circuit portion.

5. The method of claim 4, further comprising detecting secondary electrons from a plurality of circuit portions and obtaining an image of the die that represents variations in voltage across the plurality of circuit portions.

6. The method of claim 2, wherein using the electron beam includes pulsing the beam, and wherein analyzing the die includes obtaining a waveform response to the pulsed beam.

7. The method of claim 6, further comprising coupling a power supply to the die and inputting electrical signals to the die to generate a response.

8. The method of claim 1, wherein inducing a detectable response includes inducing a response as a function of an electrical characteristic of a source/drain region in the die.

9. The method of claim 1, wherein inducing a detectable response includes using a buried oxide (BOX) portion of the SOI structure as a dielectric.

10. The method of claim 9, wherein removing a portion of substrate from the back side of the semiconductor die includes exposing a portion of the BOX.

11. The method of claim 1, wherein analyzing the die includes post-manufacturing analysis.

12. The method of claim 11, wherein analyzing the die includes obtaining a response for electrical stimulus applied to circuitry in the die.

13. The method of claim 12, wherein inputting electrical signals includes inputting signals known to induce a failure in the die.

14. The method of claim 12, wherein inputting electrical signals includes inputting signals in a continuous loop.

15. The method of claim 1, further comprising inducing a detectable response from a non-defective die in the same manner as the die being analyzed, the non-defective die having the same design as the die being analyzed, and comparing the analysis of the dies.

16. A system for analyzing a semiconductor die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side, the system comprising:

means for removing substrate from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure where the substrate has been removed;

means for inducing a detectable response from the exposed region as a function of a portion of the circuitry; and

means for detecting the response and, therefrom, analyzing the die.

17. A system for analyzing a semiconductor die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side, the system comprising:

a substrate removal arrangement adapted to remove substrate from the back side of the semiconductor die and expose a region of the insulator of the SOI structure where the portion has been removed;

a probe arrangement adapted to induce a detectable response from the exposed region as a function of a portion of the circuitry; and

a detector adapted to detect the response and, therefrom, analyze the die.

18. The system of claim 17, further comprising a controller adapted to control the substrate removal arrangement.

19. The system of claim 18, wherein the controller is adapted to control the substrate removal arrangement to remove sufficient substrate to facilitate the inducing of a response from the exposed region as a function of a portion of the circuitry.

21. The system of claim 17, wherein the probe arrangement includes an SEM adapted to provide at least one of: an image of a circuit under analysis and data for probe navigation.

22. The system of claim 21, wherein the SEM also includes the detector and is further adapted to obtain an image of the die having light and dark areas, the dark areas being indicative of circuit portions having a positive voltage greater than that of lighter areas.

23. The system of claim 17, further comprising a tester adapted to introduce electrical stimulus to the die.

24. A method for analyzing a die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side, the method comprising:

removing substrate from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure where the substrate has been removed;

inputting electrical signals to the die to operate the die in a continuous loop known to cause a failure in a portion of circuitry in the die; and

directing an electron beam to the exposed region of the insulator and inducing a detectable response therefrom as a function of the portion of the circuitry failing and, therefrom, analyzing the die.

25. The method of claim 24, wherein inducing a detectable response therefrom as a function of the portion of the circuitry failing includes detecting a change in secondary electrons emitted from the exposed region of the insulator.

26. The method of claim 24, wherein directing an electron beam to the exposed region of the insulator and inducing a detectable response therefrom as a function of the portion of the circuitry failing comprises detecting a failure of the die in response to detecting an uninhibited emission of secondary electrons.

27. The method of claim 24, wherein directing an electron beam to the exposed region of the insulator and inducing a detectable response therefrom as a function of the portion of the circuitry failing comprises detecting a failure of the die in response to detecting an inhibited emission of secondary electrons.

28. A method for detecting logic states of a plurality of circuit nodes in a die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side, the method comprising:

removing substrate from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure where the substrate has been removed and adjacent to the plurality of circuit nodes;

inputting electrical signals to the die to cause the plurality of circuit nodes to take on logical states; and

scanning an electron beam across the exposed region of the insulator and inducing a detectable response therefrom as a function of the logic states of the circuit nodes adjacent to the exposed region upon which the electron beam is directed and, therefrom, detecting the logic states of the plurality of circuit nodes.

29. The method of claim 28, wherein scanning an electron beam across the exposed region of the insulator and inducing a detectable response therefrom as a function of the logic states of the circuit nodes comprises:

detecting a non-positive logical state at one of the plurality of circuit nodes as a function of detecting an uninhibited emission of secondary electrons; and

detecting a positive logical state at one of the plurality of circuit nodes as a function of an inhibited emission of secondary electrons.

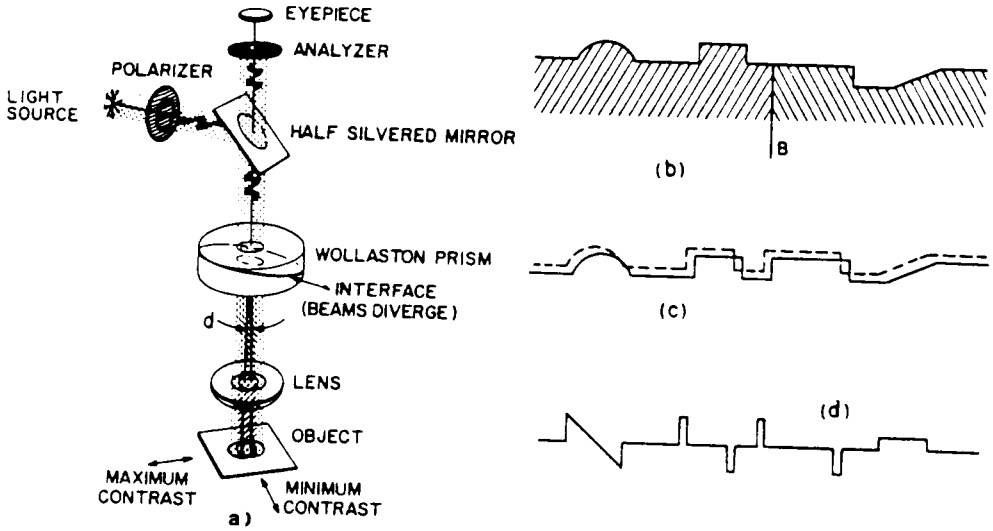

Fig. 3 (a) Features of a Nomarski interference contrast microscope operating in the reflectance mode. (b) Representation of a crosssection of a sample at a surface. (c) The wave fronts of the reflected beams after emerging from the prism, and (d) an intensity distribution in the image plane in a Nomarski interference microscope[40]. Copyright, 1983, Bell Telephone Laboratories, Incorporated, reprinted with permission.

Interference contrast is maximized when the elevation difference on the substrate is parallel to the direction of maximum displacement of the beams, and is essentially zero in the orthogonal directions. The adjustments of the polarizer, analyzer, and prism can be set to produce such maximum interference contrast. Differences in edge elevations as small as 30-50Å can be resolved with the Nomarski mode, although results do depend upon the quality of the edge. The technique is therefore used to view details on the surface of wafers, such as pits, fissures, and stacking faults that are often invisible in ordinary reflected light illumination.

Fluorescence Microscopy

In fluorescence microscopy, the wafer surface is illuminated with ultraviolet light, and in response, the illuminated materials emit characteristic radiation in the visible light regime. Organic substances fluoresce more brilliantly than the typical inorganic constituents of the wafer. The technique is therefore useful for detecting residues of photoresist and other organic films.

Television System Interface Capability

The ability to interface a microscope with a television is becoming a useful option. For example, in the wafer production environment, remote consultation (e.g. out of the clean room) can be performed, and video-tape documentation of the patterns being observed can be generated.

Scanning Electron Microscopy (SEM)

Scanning electron microscopy (SEM) has become an important tool for VLSI analysis because it has the capability of providing much higher magnification, resolution, and depth of field than optical microscopy[3,4,16]. That is, the resolution of SEM can be up to 10Å (100Å is

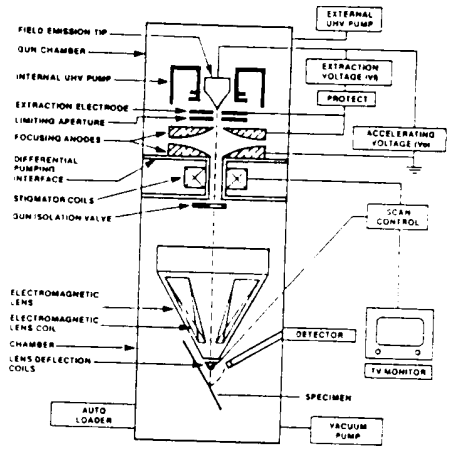

Fig. 4 Block diagram of an electron optical column of an SEM. Courtesy of Nanometrics, Inc.

routinely obtained), the magnification from 10x-100,000x (a few instruments up to 300,000x), and the depth of fields of 2-4 μm at 10,000x and 0.2-0.4 mm at 100x. (For optical microscopes the maximum resolution and magnification limits are about 1 μm [10,000 Å] and 1000x, and the depths of field are much shallower.) Note that the high depth of field makes SEM especially useful for high magnification (i.e. >2000x) examination of VLSI device surfaces, where film thicknesses rarely exceed 1 μm. SEM analysis yields information on linewidth, film thickness, step coverage, edge profiles after etch, and other morphology data.

A schematic drawing of a SEM is shown in Fig. 4. A source is used to create a beam of electrons that is accelerated to energies of 500 eV-40 keV, focused to a small diameter, and directed at the surface of a sample in a raster-scan pattern. The electrons striking the surface cause a number of physical phenomena to occur, the most important for SEM applications being

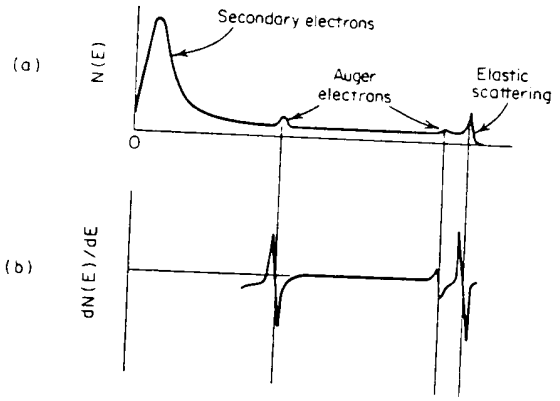

Fig. 5 (a) Energy spectrum of electrons emitted from a surface bombarded by an electron beam. (b) The derivative of the number of emitted electrons with respect to the energy.

the emission of electrons and x-rays. The emitted x-ray signal is useful for chemical analysis, and this is discussed in the section on XES.

Figure 5a shows the energy spectrum of electrons emitted from a surface bombarded by an electron beam. We that see there are three predominant types of emitted electrons: *lower energy electrons* of 0-50 eV, peaking at about 5 eV; *higher energy electrons*, with energies close to those of the primary beam electrons; and *Auger electrons*. The lower energy electrons are called *secondary electrons*, and they are produced by inelastic collisions of the primary beam and the inner shell electrons of the sample atoms. Because they possess such low energies, only secondary electrons created close to the surface actually escape and are detected. *Note that it is these low energy secondary electrons which are generally the most useful for morphology studies of VLSI.* The higher energy emitted electrons are those that have suffered *elastic* collisions with target atoms and thus still possess most of their incident energy. These are referred to as *backscattered electrons*. The mechanism by which *Auger electrons* are produced is described in a later section.

As we shall also see in later sections, the incident electrons undergo multiple collisions as they penetrate the sample, and those that are not backscattered finally come to rest after traversing a range, R (Fig. 6). The electron trajectory also changes with each collision, causing the narrow beam to spread as it penetrates the sample. Because of the short escape depth of secondary electrons, compared to the penetration depth at which beam broadening becomes influential, secondary electrons exhibit better point-to-point resolution than do backscattered electrons.

The detected electron current, which can be due to secondary or backscattered electrons, but as noted is typically the former, is used to intensity-modulate the z-axis of a CRT. An image of the sample surface is produced on the CRT screen by synchronously raster scanning the CRT screen and the electron beam of the SEM.

The *contrast* of the image depends on variations in the flux of electrons arriving at the detector, and is thus related to the *yield* of emitted electrons per incident electron[7]. For secondary electrons the yield depends on the work function of the material, and is significantly higher for oxides and other wide band gap materials than for silicon. This is another important factor that makes the use of secondary electron SEM imaging so valuable for VLSI studies. That is, the effect makes metals, oxide, and silicon patterns readily distinguishable from one another when the SEM is used to produce images in this mode. The second source of contrast in secondary electron images is the dependence of secondary electron yield on surface curvature. Therefore, surfaces that differ significantly in slope can be easily distinguished. Finally, surface

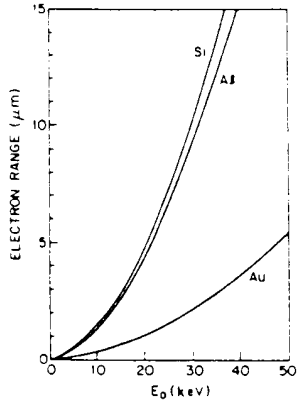

Fig. 6 The electron range in Si, Al, and Au as a function of incident beam energy[41]. Reprinted with permission of the American Physical Society.

regions that face the detector appear brighter than other surface regions[7].

The *resolution* of the SEM depends on several factors, including the type of sample under inspection and the incident beam diameter (which is dependent on the electron source, focusing optics, and accelerating voltage of the primary beam). In early generation SEMs, high voltages were required to achieve the small scanning spot sizes needed to obtain sufficient resolution for operation at high magnification. Unfortunately this leads to a problem when examining insulating surfaces. That is, when beam energies exceed the *secondary electron crossover point* (i.e. the energy at which the number of secondary electrons emitted is less than the number of incident electrons) the surface acquires excess negative charge. This then disturbs the trajectory of the incident beam, and the image is degraded. By applying a thin metallic coating to the surface of the sample (e.g. 100 Å of gold), and attaching a ground wire to the coating, an electrical path to ground is provided. This helps to reduce such charging effects. Unfortunately an Au coating makes the sample unsuitable for further processing, and this procedure is not acceptable for applications where wafers from the fab line must be inspected and returned to production (e.g. for linewidth measurement with a SEM). Another disadvantage of high accelerating voltages is that the electrons may cause damage to the circuit under inspection. Therefore SEM manufacturers have developed techniques which use accelerating voltages below the secondary electron crossover point (i.e. 800-2000 eV), and yet maintain high resolution[5].

The original tungsten hairpin electron beam sources produced beam diameters that were too large to give adequate resolution at beam energies of 1-2 keV. Thus several new sources, including the lanthanum hexaboride (LaB_6), field emission, and Schottky emitter sources have been developed to maintain high resolution at low operating voltages. Table 2 gives some characteristics of these sources[6].

The LaB_6 is very reactive and must therefore be operated at vacuum levels no greater than 10^{-7} torr. Most manufacturers of SEMs with LaB_6 sources equip the source with its own pumping system, generally using an ion pump. If properly operated, however, the LaB_6 source will last 10-50 times longer than tungsten hairpin sources.

The tungsten field emission source offers the highest brightness of these sources and the spot size can be focused to 20-50Å quite easily. The source, however, must be operated at vacuum pressures of 10^{-10} torr, which is more difficult to attain, and the maximum specimen current is approximately three orders of magnitude lower than that achieved by the other sources.

The relatively new extended Schottky field emitter source[6] provides comparable brightness to the field emission source at 1 keV, but is able to functional somewhat lower vacuums ($\sim 10^{-8}$ torr). In addition, it has a longer tip life and greater emission current stability than other electron sources. This allows Schottky emitter sources to be operated and maintained more easily than field emission sources.

SEM Voltage Contrast Microscopy

The energy distribution of secondary electrons in SEMs shows a peak at about 5 eV. These secondary electrons are collected by the detector, where their flux determines the intensity of the image. Local electric fields at the sample surface can significantly restrict the number of secondary electrons that are emitted, and such fields can be generated by applying small voltages (1-5 V) to the wafer surface. For example, if a potential difference of +5V is applied to a conductor on the wafer surface, and an electrical discontinuity exists in the conductor, the portion to which the voltage is applied will appear much darker than the section which is connected to ground (Fig. 7). Thus electrical discontinuities in long conductor lines and reverse-biased diodes can be easily located with voltage contrast microscopy techniques.

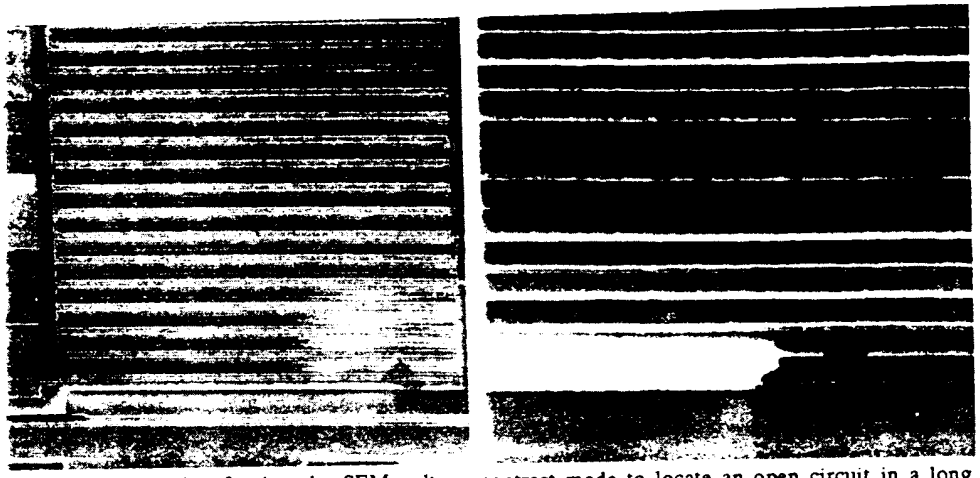

Fig. 7 Example of using the SEM voltage contrast mode to locate an open circuit in a long metal stripe. Courtesy of TRW.

Electron Beam Induced Current Microscopy (EBIC)

The difference in the amount of absorbed current by the wafer surface can modulate the intensity of the CRT image and produce enhanced contrast. Thus, this mode is useful for highlighting electrical paths, such as defects that are leakage sites in capacitors or p-n junction[10,11].

Backscattered Electron Detection

Although the detection of secondary electrons is the primary mode in which the SEM is operated, the detection of backscattered electrons has at least one useful application. Since the yield of backscattered electrons increases with increasing atomic number, Z, contrast is produced in the backscattered electron image between regions of different atomic numbers, such as aluminum particles on a silicon background.

Production SEMs and Failure Analysis SEMs

The first major application of SEMs in microlectronics was for failure analysis. Since the samples inspected in such analysis would ordinarily not be subject to further processing, they could be destructively gold coated to improve SEM image quality. Accelerating voltages and subsequent sample damage were therefore also less important. In addition, failure analysis SEMs can be designed to be equipped with auxiliary analytical capabilities such as x-ray

Table 2. CHARACTERISTICS OF ELECTRON BEAM SOURCES

Type of Emission	Tungsten Hair Pin Thermionic (Heated)	Lanthanum Hexaboride Thermionic (Heated)	Field Emission (Room Temperature)	Schottky /Extended Field (Heated)
Brightness (A /cm^2/ster)	10^4	10^5	10^8	10^8
Effective Source Size (Å)	1,000,000	200,000	100	100
Energy Spread (eV	3	3	0.2-0.3	0.28-0.38
Operating Life (hrs)	30-10	100-500	300-1000	2000-10000
Vacuum Required (torr)	10^{-3}-10^{-5}	10^{-5}-10^{-6}	10^{-9}-10^{-11}	$< 10^{-8}$

emission spectroscopy (XES). This increases their flexibility to perform a wider variety of failure analysis tasks. Finally, the time required to get samples into and out of such instruments is relatively long, making the rate of sample inspection (throughput) quite low.

As features decrease to the micron and submicron regimes, optical microscopes become less suitable for providing the resolution needed to give accurate and repeatable measurements of critical dimensions. Therefore the use of SEMs as production tools becomes more attractive. In order to make SEMs compatible with the production environment, they have to be configured differently than the traditional failure analysis instruments. Production compatible SEMs must utilize sources that can operate at low enough voltages to give high resolution on insulating surfaces (resist, oxides, etc.) without charging or damaging the wafer structures. They must also possess the ability to change samples quickly and easily (cassette-to-cassette operation) and to be able to automatically and accurately position wafers to preselected locations. Finally, since the highly trained specialist of the failure analysis staff is not likely to be available to operate such production tools, they need to be simple enough to be run by wafer fabrication personnel[8,9]. Several SEM manufacturers have produced SEMs that satisfy these requirements to some degree, but alternate linewidth measurement techniques (see Chap. 12) still predominate.

Transmission Electron Microscopy (TEM)

Just as shrinking linewidths and vertical feature sizes lead to the displacement of optical microscopes by the SEM, other VLSI applications for which the SEM had been adequate, now require an even higher resolution technique - namely TEM. Whereas maximum SEM resolutions are in the 20-30Å range, TEM offers 2Å resolution. The image in TEM is produced by the differential loss of electrons from an incident beam (60-350 keV, electron wavelength ~0.04Å) as it passes through very thin film samples. The sample must be thin enough to transmit the beam, so that essential information caused by differences in sample thickness, phase composition, crystal structure, and orientation is preserved. The limiting thickness for TEM imaging of a Si sample as a function of accelerating voltage is shown in Fig. 8. In fact, for practical VLSI analysis, the thickness is even smaller than indicated (e.g. 0.8 μm at 200 keV).

In a conventional TEM, the electron beam is focused by a condenser lens, then passes through the sample and is imaged onto a photographic plate or fluorescent screen. The *contrast* in a TEM image arises for different reasons in samples of crystalline and amorphous materials. In crystalline layers, the incident electron beam is diffracted by the materials. Abrupt changes in thickness, phase structure, or crystallographic orientation cause corresponding changes in

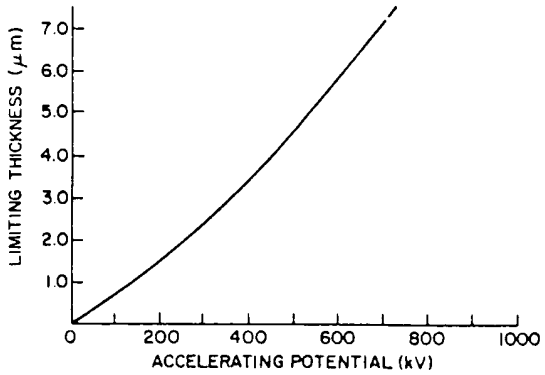

Fig. 8 Limiting thickness of a silicon sample as a function of accelerating voltage[13].

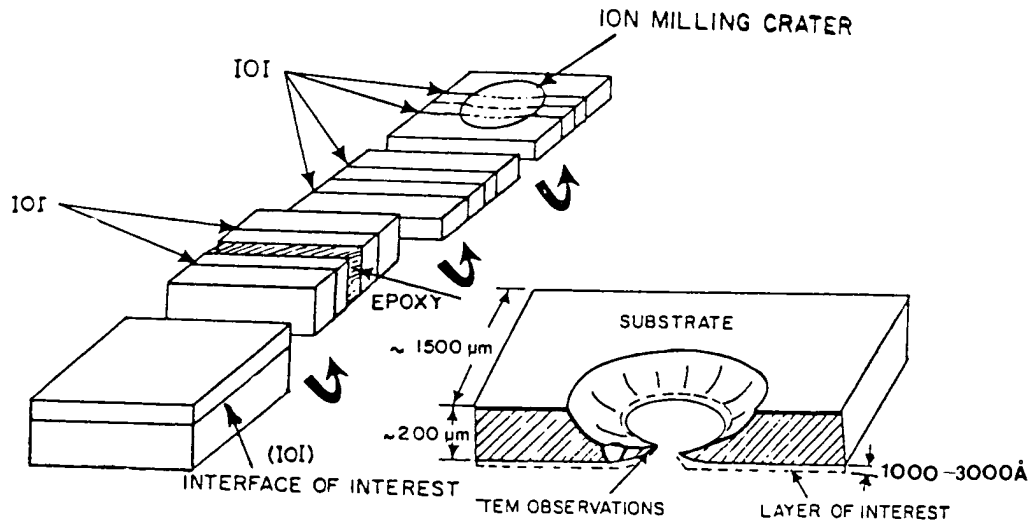

Fig. 9 Method for preparing a cross sectional sample for TEM study.

contrast, and these crystallographic features can be easily imaged at high resolution. In amorphous regions, contrast is obtained from differences in sample thickness or from differences in chemical or phase composition. TEM images from amorphous materials (e.g. oxides, nitrides) are thus somewhat easier to interpret than images from crystalline layers. Nevertheless, TEM is capable of imaging the grains of polycrystalline films, and is thus a very useful tool for measuring grain sizes and structural anomalies in thin films[12,13,14].

Sample Preparation

The two major factors that have prevented TEM from being more widely used, in spite of its excellent resolution and analytical capabilities, are: 1) the difficulties involved with preparing the required very thin samples; and 2) correctly interpreting TEM images. Related to the sample

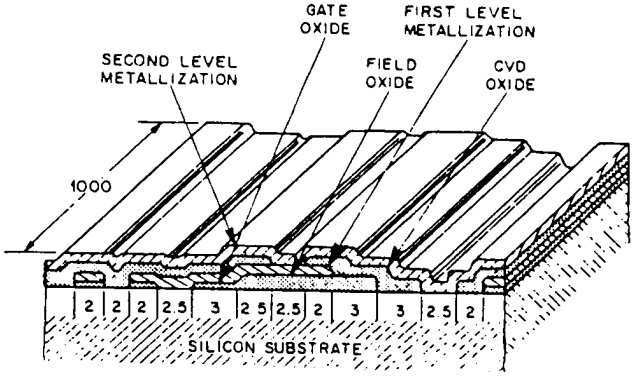

Fig. 10 Schematic of a TEM test pattern for NMOS device technology showing a 29-μm repeat unit all dimensions are in microns[40]. Copyright, 1983, Bell Telephone Laboratories Incorporated, reprinted with permission.

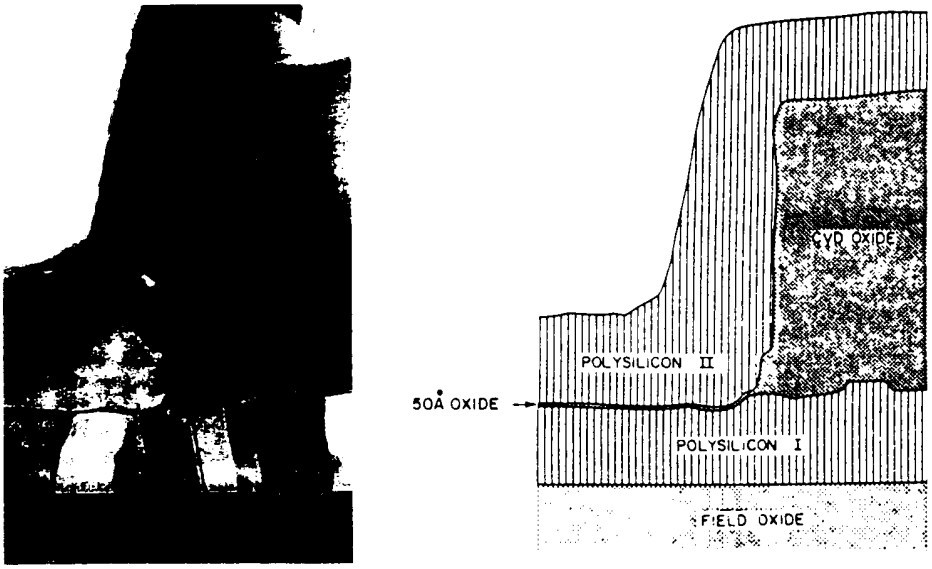

Fig. 11 TEM image and drawing of a highly resistive contact of Poly-Si II to Poly-Si I caused by the presence of a 50Å interfacial oxide. From R.B. Marcus and T T. Sheng, *Transmission Electron Microscopy of Silicon Devices and Structures,* Copyright ©, 1983 John Wiley & Sons. Reprinted with permission of John Wiley & Sons, Inc.

preparation problem, is the need to insure that the feature of interest is present within the sample region that has been thinned and prepared for TEM analysis. TEM sample sections of most interest for VLSI studies are vertical cross-sections. Such samples are prepared as shown in Fig. 9. Several hours are required to ion mill samples to the necessary thickness, making their preparation an arduous task. Details on sample preparation procedures are given in Ref. 12.

In order to help insure that the feature of interest will be present in the thinned section of the sample, a TEM test structure must be designed (as shown in Fig. 10), that will contain every morphological feature that will exist in the particular process to be fabricated. Each feature should appear within 1-3 μm in one direction, and should extend about 2 mm in the orthogonal dimension. Thus when 2 mm samples are cut from the wafer, the test structure will be present along the entire 2 mm dimension. Finally all features should be contained in ~23 μm, and this "repeat unit" should be replicated a number of times over a distance of about 2mm. Several TEM photographs appear throughout the text illustrating various applications for which TEM imaging and analysis is used (see also Fig. 11).

ELECTRON /X-RAY COMPOSITIONAL ANALYSIS TECHNIQUES

When the surface of a solid is struck by electrons or x-rays, both x-rays and electrons are emitted from the solid in response. Some of these emitted species contain energy information about elements present at the surface and in the bulk of the bombarded sample. The four analytical techniques based on the detection of such emitted x-rays and electrons are:

a) Auger Electron Spectroscopy (AES) - electron primary beam /Auger electrons are the detected species;